Politechnika Łódzka
Instytut Elektroniki

Proposal of thesis topic for mgr inż. (MSE) programme in Telecommunications and Computer Science

1. Topic: Adaptive arithmetic coder implementation in FPGA device

2. Supervisor: Piotr Wasilewski

3. Auxiliary supervisor:

4. Goals and scope of the work:

An objective of the dissertation is to design hardware architecture suitable for implementation if FPGA (Field Programmable Gate Array) device of the arithmetic coder.

First, the fixed-point version of arithmetic coder should be investigated with different adaptive schemes (in software). Next, the chosen coder should be implemented in FPGA device as the macro suitable for further use in larger projects. The design should contain both encoder and decoder.

5. Prerequisites (e.g. experience in writing programs in a computer language or knowledge of a foreign language):

Knowledge of digital logic, programmable logic devices, ability for reading technical papers, application notes and data sheets of integrated circuits, C++/Matlab basic experience

6. Literature:

Materials will be provided by the supervisor

Łódź, 2003-03-18 Supervisor's signature

THESIS TOPIC SELECTION ACKNOWLEDGMENT

Student's name:_____ Student's ID_____

Faculty: _____

Main subject/major/module: _____

Date and student's signature Supervisor's signature

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